AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application. Please ADD new claim 9 as follows:

LISTING OF CLAIMS:

1. (Previously Presented) A microcomputer comprising a memory, a central processing unit, and a functional block comprising a peripheral block, built-in said microcomputer, wherein said memory has a reprogrammable nonvolatile memory storing user data, and in which a lock code is written in a specified area; and

the microcomputer comprises:

a first decoding circuit connected with said nonvolatile memory, which reads out said lock code, and decodes said lock code;

a logic circuit that performs a predetermined operation on an externally input mode bit, by the output from the first decoding circuit; and

a second decoding circuit that decodes the processed mode bit by receiving the output from said logic circuit, and sends the obtained results to said functional block.

2. (Original) The microcomputer of claim 1, wherein said logic circuit consists of an AND circuit.

3. (Withdrawn) A microcomputer comprising a memory, a central processing unit, and a functional block comprising a peripheral block, built-in said microcomputer, wherein said memory has an internal memory comprising a reprogrammable nonvolatile memory, in which a map-selecting code for selecting a memory map is written in a specified area, and

said microcomputer comprises:

a first decoding circuit connected with said nonvolatile memory, which reads out said map-selecting code, and decodes this code;

an address decoder that decodes by a predetermined bit of an address bus, and thereby outputs a chip-selecting signal; and

a selector circuit that selects said memory map by receiving the output from said first decoding circuit and the output from said address decoder, and sends the results to said internal memory comprising said nonvolatile memory.

4. (Withdrawn) The microcomputer of claim 3, wherein said internal memory comprises a mask ROM.

5. (Previously Presented) A microcomputer comprising a memory, a central processing unit, a functional block comprising a peripheral block, built-in said microcomputer, and an external terminal, wherein said memory comprises a reprogrammable nonvolatile memory storing user data, and in which a function-selecting code for selecting the function of the external terminal is written in a specified area; and

said microcomputer comprises:

a first decoding circuit connected with the nonvolatile memory, which reads out said function-selecting code and decodes this code; and

a selector circuit that selects a function of the external terminal by receiving the output from said first decoding circuit.

6. (Previously Presented) A microcomputer comprising a memory, a central processing unit, and a functional block comprising a peripheral block, built-in said microcomputer, wherein said memory comprises a reprogrammable nonvolatile memory storing user data, and in which a limiting code for limiting a command is written in a specified area; and

said microcomputer comprises:

a first decoding circuit connected with said nonvolatile memory, which reads out said limiting code, and decodes this code; and

a second decoding circuit that limits a command to be used, by the output from said first decoding circuit.

7. (Withdrawn) A microcomputer comprising a memory, a central processing unit, and a functional block comprising a peripheral block, built-in said microcomputer, wherein said memory comprises a reprogrammable nonvolatile memory; and

said microcomputer comprises:

a voltage-regulating circuit that monitors a power supply voltage;

a logic circuit that performs a predetermined operation on an externally input mode bit by the output from said voltage-regulating circuit; and

a decoding circuit that decodes the processed mode bit by receiving the output from said logic circuit, and sends the results to said functional block.

8. (Original) The microcomputer of claim 1, wherein said reprogrammable nonvolatile memory consists of a data memory and a program memory.

9. (New) The microcomputer of claim 1, wherein the logic circuit masks the input mode bit by the decoded lock code.